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Design and Simulation of an Optimized QCA-Based Half Adder Using Bistable Quantum Cells

Manisha Muvel [1], C. K. Tiwari [2], Dr. Jay Tiwari [3], Dr. Dev Kumar Rai [4]

Abstract

Quantum-dot Cellular Automata (QCA) is an emerging nanotechnology that offers a potential alternative to conventional CMOS-based digital logic by enabling ultra-dense, low-power computational architectures. This paper presents the design and simulation of a novel half adder using QCA technology, employing bistable quantum cells to enhance circuit efficiency and reduce area and latency. The proposed design aims to improve upon traditional logic gate implementations by minimizing complexity while maintaining functional accuracy. Simulations are conducted using QCA Designer to validate the structure's performance in terms of area, cell count, and delay. The results confirm the feasibility of the design for next-generation nanoelectronic applications in arithmetic logic circuits.

Keywords: Quantum-dot Cellular Automata (QCA), Nanoelectronics, Half Adder, Quantum Cells, Low-Power Design, Bistable Vector.

[1,2] *Department of Electronics & Communication, Patel College of Science and Technology, Indore (M.P.), India*
[3,4] *Patel College of Science and Technology, Indore (M.P.), India*

I. INTRODUCTION

The limitations of traditional CMOS technology, such as power dissipation, physical scaling constraints, and increasing fabrication costs, have driven research toward alternative computing paradigms [1-5]. Quantum-dot Cellular Automata (QCA) has emerged as a promising nanotechnology that utilizes the position of electrons within quantum dots to encode binary information, eliminating the need for current flow in traditional transistors [6-8]. The fundamental building block in QCA is the quantum cell, which operates based on Coulombic interactions, offering the potential for ultra-low-power and highly dense circuits [9].

QCA presents a significant advantage in designing combinational and sequential circuits at the nanoscale, making it a viable candidate for future computing systems [5, 9, 10-12]. Among the basic components required in arithmetic logic units, the half adder plays a crucial role in performing binary addition. This

study proposes a novel design of a QCA-based half adder using bistable quantum cells to achieve optimal performance with reduced area and propagation delay. The design is simulated using QCA Designer software, and the outcomes are analyzed in terms of efficiency and scalability. This paper contributes to the ongoing development of reliable and efficient QCA architectures for nanoscale digital logic [13].

Quantum dots are nanostructures created from standard semi-conductive materials such as Si/SiO_2. These structures can be modelled as 3-dimensional quantum wells. Its structures are constructed as an array of quantum cells within which every cell has an electrostatic interaction with its neighbouring cells [12, 14-16]. It consists of four metal islands (conductors) that constitute what are known as quantum dots. It's positioned at the corners of a square. QCA based circuits have the advantage of high speed, high integrity and low power consumption. Also Q QCA circuits have the advantage of high parallel processing [17-18].

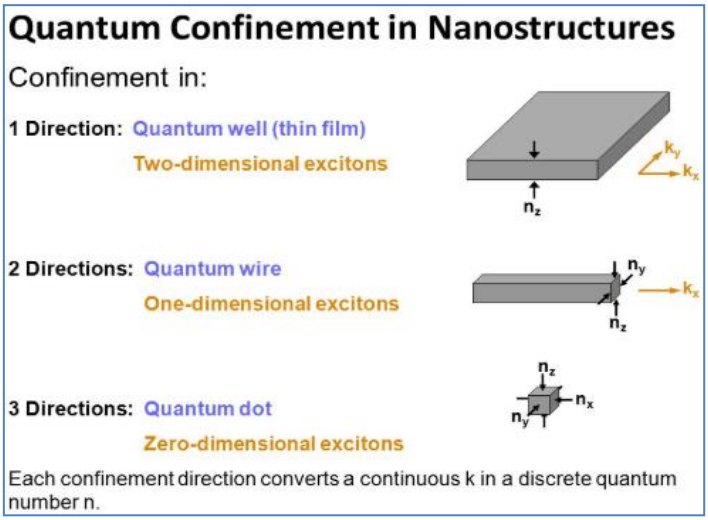


Fig. 1: Quantum Configuration in Nano-strictures

It comprises four or five nanometer-sized quantum dots, in which electrons may be confined, due to their unique electronic and optical properties. The each cell contains two extra mobile electrons, which are allowed to tunnel between neigh-boring sites of the cell or (free electrons that can move between the dots) [6]. The four quantum dots form a QCA cell with one electron each in two of the four dots occupying "diametrically opposite" locations [6]. Electrons occupy opposite (diagonal) corner quantum-dots because Coulomb repulsion is less compared to the scenario when they are in adjacent quantum dots.

Nanotechnologies are the design, characterization, production and application of structures, devices and systems by controlling shape and size at nanometer scale." The nanometer scale the nanometer scale is conventionally defined as 1 to 100 nm. One nanometer is one billionth of a meter (10^{-9} m).

II. Quantum Dot Cell

The new computing paradigm, Quantum-dot Cellular Automata (QCA), has been extensively studied in recent years. The fundamental building block of QCA is a 'cell,' which consists of four quantum dots (QDs) positioned at the corners of a square. These dots hold two mobile electrons that can tunnel between the dots within the cell but not between adjacent cells. The arrangement and interaction of these electrons define the cell's polarization, which represents binary information. This structure enables QCA to perform logic operations without the need for traditional current flow, offering a highly compact and energy-efficient alternative to conventional CMOS technology. The new computing paradigm, Quantum Dot Cellular Automata has been extensively studied in recent years [7]. The basic element in Quantum dot cellular automata is a "cell" that consists of four metal islands dots known as QD. It's positioned at the corners of squared cell and two free charges [19-20].

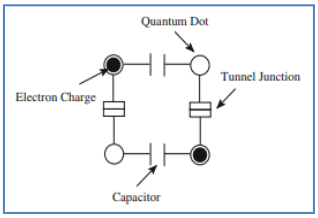


Fig.2: QCA Cell

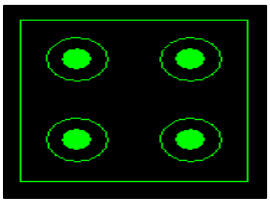


Fig. 3: Empty cell (P=0)

Fig.4: Quantum-dots 90° cells polarizations

III. Elements of QCA

The basic elements for QCA logic circuit design are wire, inverter, and 3-input majority gate. The QCA wire is formed by an array of quantum cells shown in Figure 5, The QCA inverter is built by placing quantum cells structure shown in Figure 6, it is a simple device that inverts an input signal. The majority voter (MV) consists of four QCA cells around a centre QCA cell, of only three input QCA cells and one output cell. Where A, B and C are input and F is the output as shown in Figure 7.

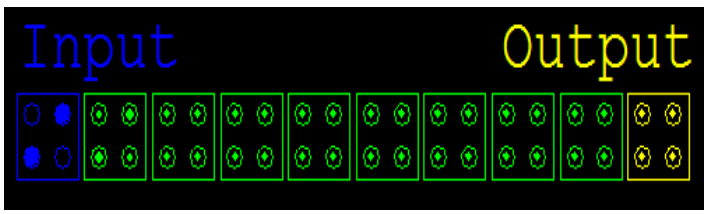


Fig. 5: Layout of QCA Wire

Table 1: Truth Table for QCA Wire

Input	Output
Normal cell for 90^0	
0	0
1	1
Rotate cell for 45^0	
0	1
1	0

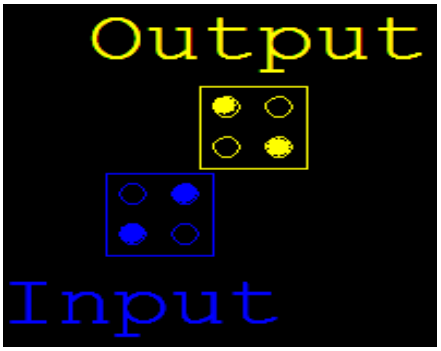
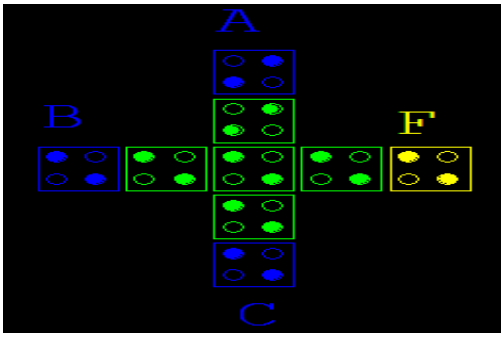


Fig. 6: Layout of Inverter



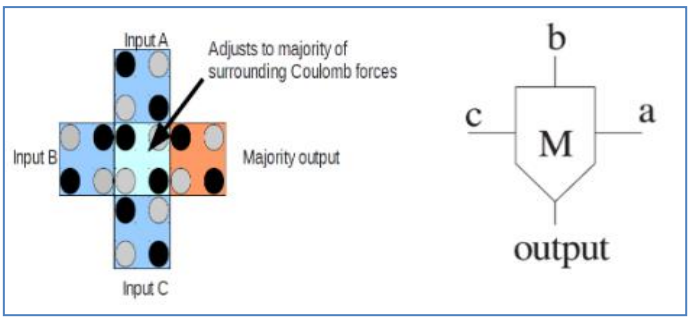


Fig. 7: Layout of majority voter (MV) and its symbol

IV. HALF ADDER

The half adder is a fundamental combinational logic circuit used to perform the addition of two single-bit binary numbers. It has two inputs, typically labeled A and B, and two outputs: Sum (S) and Carry (C). The Sum output is obtained by performing the XOR operation on inputs A and B, while the Carry output is generated by the AND operation of the same inputs. Although the half adder is limited to adding only two bits without accounting for carry-in from a previous stage, it serves as a basic building block for designing more complex arithmetic circuits such as full adders and arithmetic logic units.

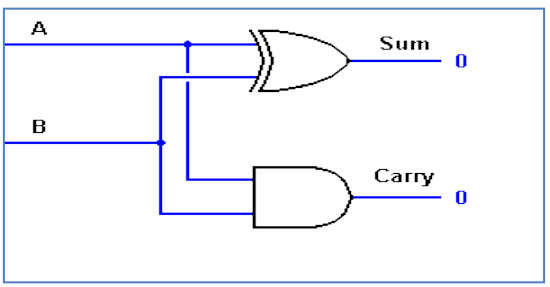


Fig. 8: Half Adder Circuit

Table 2: The truth table of the half adder

Inputs		Outputs	
A	**B**	**Sum**	**Carry**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Then the Boolean expression for a half adder is as follows.

For the SUM bit:

$$SUM = A\,XOR\,B = A \oplus B \qquad (1)$$

For the CARRY bit:

$$CARRY = A\,AND\,B = A.B \qquad (2)$$

V. SIMULATION OF HALF ADDER

To design and verify the proposed circuit layout and functionality, the QCA Designer simulation tool (version 2.0.3) is used. The simulation parameters are configured for bistable approximation with the following settings: cell size = 18 nm, clock high = 9.8×10^{-22} J, clock low = 3.8×10^{-23} J, quantum dot diameter = 5 nm, and cell spacing = 2 nm. In this study, the half adder circuit performs the addition of two Boolean inputs and produces two outputs: Sum and Carry. The proposed QCA-based half adder design, illustrated in Figure 9, consists of 47 quantum cells, occupies a layout area of 50,208.35 nm², utilizes a single-layer design, and operates with a clock cycle delay of one.

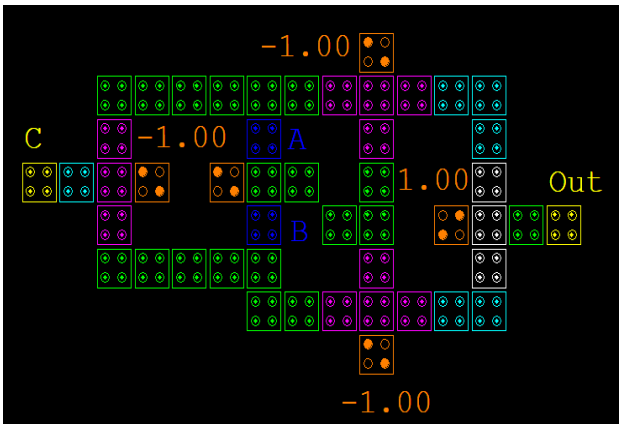


Fig. 9: layout design of QCA Half Adder circuits

This design is efficient in team of design cell area as well as used cell count. The proposed design compared to previous design as shown in table 3 and simulation result is shown in figure 10.

Table 3: Comparative results of the Proposed Design and previous designs of Half Adder

Layout design	QCA Cells	Area (μm^2)	Delay
PROPOSED DESIGN			
QCA Half Adder	47	0.05	1
PREVIOUS DESIGN			
Peer Zahoor et al.	62	0.08	2
S. Karthigai Lakshmi et al.	77	0.083	1
Peer Zahoor Ahmad et al.	107	0.12	2.5

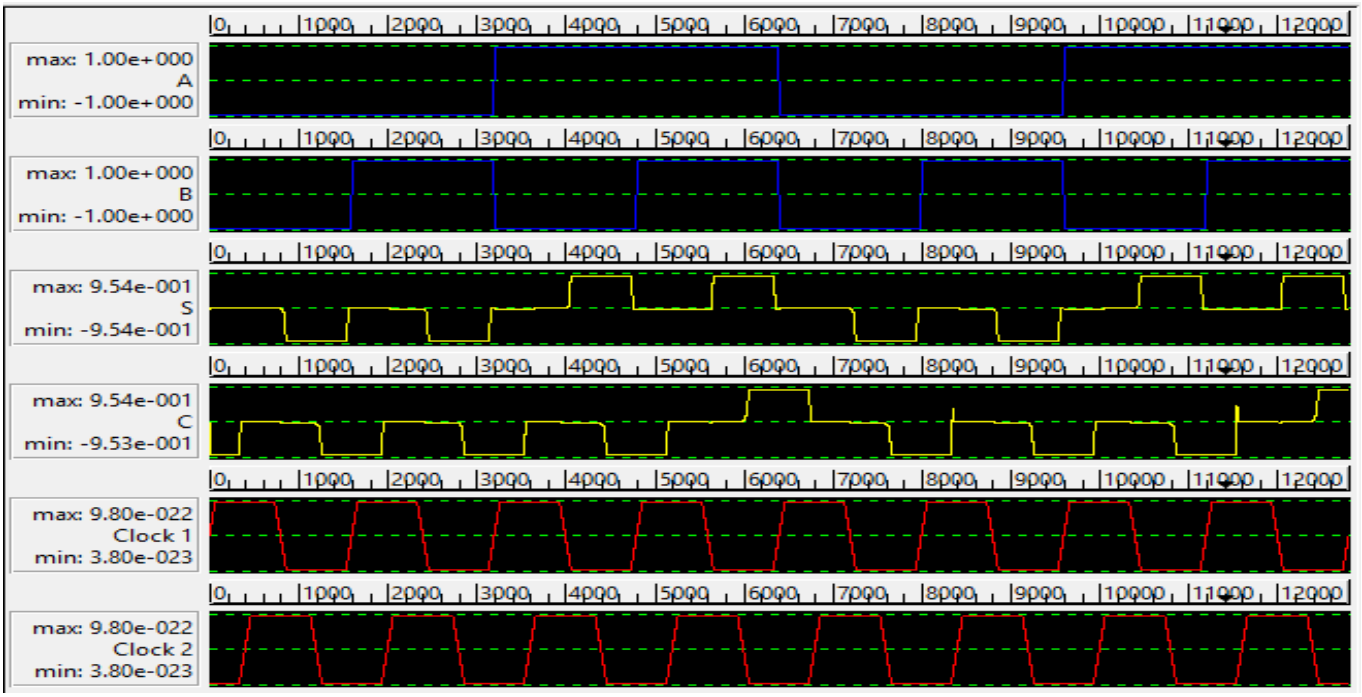


Fig. 10: Simulation results for QCA Half Adder

VI. CONCLUSION

In this paper, a novel half adder design using Quantum-dot Cellular Automata (QCA) was proposed and simulated using QCA Designer version 2.0.3. The simulation results were validated against the standard digital truth table, confirming the correct functionality of the circuit. The proposed design demonstrates improvements in terms of reduced complexity, compact design area (50,208.35 nm²), and minimal clock cycle delay (one cycle). Additionally, the design utilizes only 47 quantum cells with a single-layer architecture, making it a promising candidate for future nanoscale computing systems. Comparative analysis with existing designs highlights the efficiency and optimization achieved in the proposed half adder implementation.

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